

## SEQUENCE-BASED VERIFICATION METHOD AND SYSTEM

### ABSTRACT

A hardware verification method includes obtaining a set of packets to be driven by a device under test and obtaining a set of timing and relation criteria which determines a sequence in which the packets should be driven by the device under test.

- 5 The method further includes starting multiple drive loops, each drive loop picking up a packet and forcing the device under test to drive the packet. The method further includes starting multiple expect loops, each expect loop determining when to expect a packet driven by the device under test and picking up the expected packet when it arrives. For each drive loop, the method confirms that the timing and relation criteria
- 10 are satisfied prior to allowing the drive loop to force the device under test. For each expect loop, the method checks if the expected packet arrives within a specified time period and raises an error flag if the expected packet does not arrive within the specified time period.

06145.012001.20010109.01.doc

06145.012001.20010109.01.doc